EE/CprE/SE 492 WEEKLY REPORT 2

2/13/25 - 2/27/25

sdmay25-16

Project title: Multi-Channel High-Gain Low Noise Amplifier for High-Frequency Ultrasound Signal Acquisition

Client &/Advisor: Manojit Pramanik

Team Members/Role:

Jon Wetenkamp, Yash Gaonkar, Ethan Hulinsky, Ryan Ellerbach

- **Bi-Weekly Summary:**
- During the Last week we continued with our individual goals. The major things we completed in the last two weeks include finishing the schematic, completing most of the Layout and finishing component selection. We also decided how we are going to implement EM shielding using a faraday cage around each stage and a copper layer with plenty of vias to ground around the whole board.
- **Past week accomplishments**
    - Yash Gaonkar: Researched EM shielding compatible with the new design. Finalizing the faraday cage being used for the design
    - Ethan Hulinsky: Routed signal paths by introducing a gap into the EM shielding footprint, calculated trace widths for 50 ohm impedance matching and updated layout.
    - Ryan Ellerbach: Finished creating footprints for components that will be used in the PCB design. Researched EM shielding effect on traces and components, board thickness, and component spacing.
    - Jon Wetenkamp: Finished up work on the schematic. Might need minor changes in the future, but the first schematic should be done. Copied layout of channel 1 to remaining channels, created layout for single stage channels.

- **Pending issues**

  1) We are still working on the EM shielding and are going to confer with our project contact to figure out specifics

  2) The team needs to figure out the specifics of components spacing as well as board thickness.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**

Jonathan Wetenkamp	Finished up work on the schematic. Copied layout of channel 1 to remaining channels, created layout for single stage channels.	4	34.5
Yash Gaonkar	Researched EM shielding compatible with the new plan for board layout.	3	31.5
Ryan Ellerbach	Finished creating footprints for components that will be used in the PCB design. Researched shielding, PCB thickness, and component spacing.	4.5	37
Ethan Hulinsky	Routed signal paths by introducing a gap into the EM shielding footprint, calculated trace widths for 50 ohm impedance matching and updated layout.	4	36

- **Plans for the upcoming week**

Meeting with our project contact to show what we have so far for the design and ask a few questions. After meeting with him we will adjust our design, put on the finishing touches, and order the parts and boards.